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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,917	02/13/2002	Kenneth Elmon Koch III	46872.269148 (UNCC 2001-0	1717

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,917	KOCH, KENNETH ELMON	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/16/06,04/17/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 9-27* is/are pending in the application.

4a) Of the above claim(s) *2 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 9-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/02 (blank form), 10/28/05*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-27 remain for examination. Claims 28-45 have been canceled.

2. The IDS on 10/28/05 has been received and considered. Examiner thanks applicant for clarifying the IDS blank 1449 form on 02/13/02.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/803,690. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

4. Although the copending claim 1 did not recite the Conjunctive normal form Boolean expressions as claimed , the copending claim 1 recited normal form Boolean expressions. It would have been obvious to one of ordinary skill in the art to include conjunctive form as claimed because one of ordinary skill in the art should be able to recognize the normal form Boolean expression was also applicable in conjunctive form in order to expand the logic structure of the Boolean operations because the conjunctive form (e.g. the AND) was one of the standard format of the Boolean

expression (the other format would be OR, XOR, etc), and in doing so, provided a motivation

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saldanha et al. (5,682,519) in view of Serlet (4,792,909).

6. As to claims 1, 21, Saldanha taught a processor comprising at least :

a) a Boolean logic circuit (see fig.5) , wherein the Boolean logic unit is operable for performing the short circuit evaluation of Conjunctive Normal Form Boolean expressions/operations (see AND gate, see the short circuited AND in col.7, lines 53-65, see for Boolean expression);

b) a plurality of input/output interfaces (see fig.5) , wherein the plurality of input/output interfaces are operable for receiving plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results, and a plurality of registers (see Boolean expressions and compiled result in col.4, lines 48-67, col.5, lines 1-57, see also figs.4 , 7,8 for the input/output connections, see also the

simulation of logic properties of the circuit and the Boolean expressions in col.2, lines 36-67 for background).

7. As to the newly amended feature of "dynamically" performing short circuit evaluation in claim 1, Saldanha also taught that his system was run on Sun Unix operating system , and the low power synthesis module (see algorithm used for low power short circuit in col.5, lines 60-67, col.6, lines 1-14) was part of Sequential Interactive System software (see col.5, lines 45-52). Form the above , it can be seen easily that Saldanha's short circuit evaluation (for purpose of low power) was based on interactive software, and an interactive software , as already known in the art, was able to respond whenever the user's request occurred, and therefore, it was dynamic. Saldanha did not explicitly characterize his system as "dynamic", but due to the interactive nature of the software, it was dynamic.

8. As to the amended static feature in claim 1, Saldanha did not specifically show that his Boolean circuit was static as clamed. However, Serlet taught a system for generating a static Boolean circuit (see col.2, lines 38-42, see also col.5, lines 20-68, col.6, lines 1-32 for the details of the combinational logic of the CMOS circuit). It would have been obvious to one of ordinary skill in the art to use Serlet in Saldanha for including the Boolean static circuit as claimed because the use of Serlet could provide Saldanha the ability to replace the circuit elements with alternative logic gates, such as a static circuit, and therefore increasing the ability to adaptability of the system,

and because Saldanha also taught a CMOS combinational logic circuit in the background art, which provided the background teaching of Saldanha, and was a suggestion of the applicability of the Boolean static circuit, such as CMOS, into Saldanha in order to enhance the adaptability of Saldanha, and it could be readily achieved by predefining the static logic circuit of Serlet into Saldanha's configuration file with modified control parameters, such as the R/W port and the circuit type, so that specific Boolean static gates of Serlet could be recognized by Saldanha, and for doing so, provided a motivating.

9. As to amended claim 3, 9, Saldanha also taught the composite results of all AND computations in the evaluation of the Conjunctive Normal Form Boolean expression/operation were stored and represented be an a-bit AND register(see the evaluation of conjunctives AND result in fig.5, see also the OR conjunctives results in fig.5)

10. As to claims 4,5, Saldanha also had default and initialized to a default value (see "1" in fig.4).

11. As to claim 6, Saldanha also remained one on true result (see the AND B value of 1 in col.2, line 62, see the OR 1 value in col.2, line 63, see also figs.5,7).

12. As to claim 7, see short circuited AND "0" in figs.5,7).

13. As to claims 10, 11,12, Saldanha also included OR "zero" until the conjunct was "one" (see figs.5,7, see also the enable signal in fig.5).

14. As to claim 13, Saldanha also included conjunct evaluation to true if the OR register is set to a value other than the default and the OR conjunct register is set to value other than the default, and the processor short-circuits to the start of the next conjunct (see the short circuited OR in col.7, lines 27-41, see the iterations for the next conjunct).

15. As to claim 14,15, Saldanha also included a decoder (see the AND , OR, and the branches jumps for the conditional jump in fig.7).

16. As to claim16, Saldanha also inputted in parallel (see input at 560 in fig.8, see also the background of encoding in col.1, lines 63-67) and outputted across a device bus either in series (see bus to 600) or parallel (see parallel inputs to (500).

17. As to claim 17, see RAM in fig.2.

18. As to claims 18,19, 20, a micro program and program counter not explicitly shown, but see the computer OS, and software in col.5, lines 40-52). No specific format of the micro program and program counter can be found in the claim, therefore, it is read as a micro program and a program counter in the computer in general. AS to the configuring of the program counter and the jump operations , no specific configuration of the program counter and the jump operations has been reflected into the claim, therefore, it is assumed to be a general configuration. Saldanha also taught many computer system type and configurations were suitable for use (see col.5, lines 54-56).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saldanha et al. (5,682,519) in view of Serlet (4,792,909) as applied to claim 1, 21 above, and further in view of Gupta (6,385,757) .

20. As to clams 22,23,25, limitations of claims 1,21 have already discussed in paragraph above, therefore it will not be repeated herein. Saldanha did not specifically showed the instruction register, address register, nor the 3 bit operation code as clamed. However, Gupta disclosed a system including an instruction register , address register, and a variable length instruction (see col.44, lines 43-61, see also fig.14). It would have been obvious to one of ordinary skill in the art to use Gupta in Saldanha for including instruction register and the 3 bit operation code as claimed because the use of Gupta could provide Saldanha the ability to adapt to different instruction width based on the system requirement, and Saldanha did disclose that many computer system types and configuration were suitable for his system (se col.5, lines 54-57), which was an indication of the applicability of different system configurations, such as different numbered o of opcode width , into the system in order to provide the enhanced adaptability, and for doing so, provided a motivation.

21. As to claim 24, see the instruction sequencer for the memory address in col.10, lines 16-28 for the address register. See also the OR in Saldanha for the OR register.

22. As to claims 26,27, as to the single bit register, Gupta already taught a variable length register, therefore, a single bit, or any number of bit should be recognizable by one ordinary skill in the art for implementing the logic gate operations.

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Mansfield , Jr. et al. (5,530,939) is cited for the background teaching of the short circuited evaluation of the Boolean AND and OR (see col.5, lines 26-44);

b) Poirot (5,805,462) is cited for the teaching of the evaluation of the Boolean logic circuit (see col.5, lines 1-40, col.5, lines 25-60).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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21 Century Strategic Plan

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